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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/031,445	01/22/2002	Akira Asai	740819-734	6739

7590 05/21/2003

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EXAMINER

GEBREMARIAM, SAMUEL A

ART UNIT	PAPER NUMBER
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2811

DATE MAILED: 05/21/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Applicati n No.

10/031,445

Applicant(s)

ASAI ET AL.

Examiner

Samuel A Gebremariam

Art Unit

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-- The MAILING DATE of this communication appears on the cover sheet with th correspondence address --

Period f r Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 07 March 2003.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-5 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-5 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 04 April 2002 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☒ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 4.5. 6) ☐ Other:

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of group I, claims 1-5 drawn to a semiconductor device in Paper No. 7 is acknowledged.

Drawings

2. Applicant is required to submit a proposed drawing correction in reply to this Office action. However, formal correction of the noted defect can be deferred until the application is allowed by the examiner.
3. Figure 10 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g).

Specification

4. The disclosure is objected to because of the following informalities: page 2, line 26 call attention to reference numeral "511", which does not exist in the drawings; on page 20 line 16 and 17 call attention to reference numeral "122" as second deposited oxide; reference numeral "512" in the specification is not identified in figure 10. Page 1 line 18, the phrase "an SiGe" is incorrect. Further applicant is recommended to go through the specification to correct such minor grammatical errors.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.
6. Claim 3 recites the limitation "said underlying insulator film" in line 14. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

Claims 1, 2, 4 and 5 are rejected under 35 U.S.C. 102(e) as being anticipated by Sato, JP patent No. 200058555A.

Regarding claim 1, Sato teaches a bipolar transistor (fig. 1b), comprising: a first semiconductor layer to be a collector layer (3) formed on a substrate (1) and including an impurity of a first conductive type (n); a second semiconductor layer to be a base layer (9) formed on the first semiconductor layer and including an impurity of a second conductive type (p); a third semiconductor layer (11) formed on the second semiconductor layer from a material having a bandgap different from a bandgap of the second semiconductor layer; an insulator film (13) provided on the third semiconductor layer (11); an opening portion (103) formed through the insulator film to reach the third semiconductor layer; and an emitter connecting electrode (18) made of a conductor material and brought into contact with the third semiconductor layer by filling the opening portion in the insulator film, wherein the third semiconductor layer includes an emitter diffusion layer of the first conductive type positioned below the opening portion, and a peripheral layer (14) including the impurity of the second conductive type at least in an upper part thereof at a region located at a side of the emitter diffusion layer.

Regarding claim 2, Sato teaches (fig. 1b) the entire claimed structure of claim 1 above including the insulator film (13) is formed from a silicon dioxide film doped with the impurity of the second conductive type (BSG, see English abstract); and the impurity of the second conductive type included in at least a part of the top portion of the third semiconductor layer is the impurity of the second conductive type out-diffused from the insulator film.

Regarding claim 4, Sato teaches (fig. 1b) the entire claimed structure of claim 1 above including the impurity of the first conductive type in the emitter diffusion layer of the third semiconductor layer is the impurity of the first conductive type out-diffused from the emitter connecting electrode (18).

Regarding claim 5, Sato teaches (fig. 1b) the entire claimed structure of claim 1 above including the substrate is a silicon substrate (1); the first semiconductor layer is an silicon layer (3); the second semiconductor layer is a SiGe layer (9); and the third semiconductor layer (11) is a silicon layer.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. References A-C are cited as being related to heterojunction bipolar transistors.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Samuel Admassu Gebremariam whose telephone number is 703 305 1913. The examiner can normally be reached on Monday-Friday.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 703-308-2772. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Samuel Admassu Gebremariam
May 15, 2003

RECEIVED
MAY 15 2003
Steve Lake